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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/731,566	12/08/2003	Gilbert C. Vandling	6450.P003	5068

8791 7590 12/12/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

BL

Office Action Summary	Application No.	Applicant(s)	
	10/731,566	VANDLING, GILBERT C.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 January 1934*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-13,21-24 and 26-29* is/are rejected.

7)☒ Claim(s) *9,14-20,25 and 30-34* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/15/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10731/566, and amendment filed on 9/30/2005. Claims 1-34 remain pending in the application.

2. The response to restriction and election is acknowledged.

Drawings

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-8, 10-12, 21-24 and 26-28 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (US 2003/0154433 A1).

6. As to claims 1 and 21, Wang et al. teach a design method for transforming sequential logic design into equivalent combinational logic (Fig. 2, 17-19, summary) comprising simulating each stage of a clocking sequence to produce simulation values

and saving the simulation values and performing a plurality of backward logic traces based on the saved simulation value to provide an equivalent combinational logic representation of sequential logic design (0011 describes that the invention is used to generated a broadcast scan patterns that are applied to the scan cells (memory elements) of an IC design under test. This process converts the virtual scan patterns stored in an ATE into broadcast scan patterns that are applied to the package scan input pins of the IC using a broadcaster. The broadcast maps the virtual scan patterns into their corresponding broadcast scan patterns that are used to test for various faults, such as stuck-at faults, delay faults, and bridging faults in an IC. The ATE performs simulation to produce and storing simulation values. Backtracking logic traces on any shift clock cycle is described in 0015. Figs. 17-19 show a transform model that transforms a sequential logic design into an equivalent combinational circuit. 0013 describes combinational equivalent circuit).

7. As to claim 5, Wang et al. teach a design method for transforming sequential logic design into equivalent combinational logic (Figs. 2, 17-19, summary) comprising simulating each stage of a clocking sequence to produce simulation values and saving the simulation values and performing a plurality of backward logic traces based on the saved simulation value to provide an equivalent combinational logic representation of sequential logic design (0011 describes that the invention is used to generated a broadcast scan patterns that are applied to the scan cells (memory elements) of an IC design under test. This process converts the virtual scan patterns stored in an ATE into broadcast scan patterns that are applied to the package scan input pins of the IC using

a broadcaster. The broadcast maps the virtual scan patterns into their corresponding broadcast scan patterns that are used to test for various faults, such as stuck-at faults, delay faults, and bridging faults in an IC. The ATE performs simulation to produce and storing simulation values. Backtracking logic traces on any shift clock cycle is described in 0015. Figs. 17-19 show a transform model that transforms a sequential logic design into an equivalent combinational circuit). In addition, Wang et al. teach simulation a scan operation (generation of broadcast scan patterns, at least see 0014).

8. As to claims 2-4 and 22-24, Wang et al. tracing backwards to all cone inputs (scan cell outputs) from each cone output (scan cell input) and then to use a maximum covering approach to reorder all cone input (scan cell outputs) so that only on constrained scan cell is located in a single broadcast channel during any shift clock cycle; 0015). Wang et al. also teach creating and generating of broadcast scan patterns that meet input constraints imposed by the broadcaster (0014).

9. As to claim 6, Wang et al. teach the broadcaster consists of a virtual scan controller having a 3-stage shift register, a combinational logic network and an optional scan connector (0063). The purpose of applying virtual scan input values is to change and store a proper set-up value combination in the virtual scan controller (0064) (setting control inputs to their scan-enable values).

10. As to claims 7-8, Wang et al. teach transforming a sequential circuit into a combinational equivalent circuit and performing combinational fault simulation (0096). Wang et al. his invention involves a broadcast scan chain reordering step before ATPG takes place. Our approach is to perform input-cone analysis form each cone output

(scan cell input) tracing backwards to all cone inputs (scan cell outputs) and then use a maximum covering approach to reorder all cone inputs so that only one constrained scan cell located on a single broadcast channel during any shift clock cycle. These broadcast scan order constraints reduce the data dependency among broadcast channels associated with on ATE output. This gives the ATPG tool to a better chance of generating broadcast scan patterns that achieve the target fault coverage without having to use a different set of input constraints (0015-0016). These teachings suggest that in order to perform the simulating stage, all clocks must be turned off (simulating equivalent combination circuit); and when given clock is pulsed, turning off all other clocks (allowing only one constrained scan cell to be located on a single broadcast channel during any shift clock cycle).

11. As to claims 10 and 26, Wang et al. teach transforming a sequential circuit into a combinational equivalent circuit and performing combinational fault simulation (0096). Wang et al. his invention involves a broadcast scan chain reordering step before ATPG takes place. Our approach is to perform input-cone analysis form each cone output (scan cell input) tracing backwards to all cone inputs (scan cell outputs) and then use a maximum covering approach to reorder all cone inputs so that only one constrained scan cell located on a single broadcast channel during any shift clock cycle. These broadcast scan order constraints reduce the data dependency among broadcast channels associated with on ATE output. This gives the ATPG tool to a better chance of generating broadcast scan patterns that achieve the target fault coverage without having to use a different set of input constraints (0015-0016).

12. As to claims 11-12 and 27-28, Wang et al. partitioning the design in to scan partitions and processing of smaller pieces on separately (0012).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 13 and 29 are rejected under 35 U.S.C. 103(a) as being obvious over Wang et al. (US 2003/0154433 A1) in view of Allen (5,878,055).

15. As to claims 13 and 29, Wang et al. do not teach using one or more chopped clocks. Allen teaches using clock choppers to delay various clock edges in order to reduce or eliminate early mode failures in the final design (col. 2 lines 7-29). With such motivation and expected result, it would have been obvious to practitioners in the art to have included one or more chopped clocks in the sequential design.

Allowable Subject Matter

16. Claims 9, 25, 15-20, 30 and 31-34 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

17. The prior art of record does not teach or fairly suggest simulating primary input force events by turning off all of the clock inputs to the design and the operation of performing a plurality of backward traces as recited in claims 15 and 31.

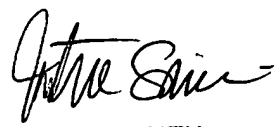
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek



VUTHE SIEK
PRIMARY EXAMINER